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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,030	08/29/2003	Paul J. Garnett	5681-70900	1562

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EXAMINER	
PEZZLO, JOHN	
ART UNIT	**PAPER NUMBER**
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/653,030	GARNETT ET AL.	
	Examiner	Art Unit	
	John Pezzlo	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

I. Claims 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Zadikian et al. (US 6,724,757 B1) hereinafter Zadikian.

1. Regarding claim 1 – Zadikian discloses a plurality of shelves, refer to Figure 4, each shelf having a carrier for removably receiving a plurality of information processing modules (line cards and shelf processor cards, refer to Figure 4) and a switching module, SM420 in Figure 4), and an interconnection member (backplane, column 13 lines 18 to 36) for providing connections between the information processing modules and the switching module, wherein the switching modules of the respective shelves are interconnected in a logical stacking configuration to form a logical stacking arrangement, refer to Figures 1A, 2-4 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36. Radian discloses a rack with comprises shelves and a backplane within each shelf comprises line cards, processor cards, and switch

cards. The cards are interconnected to provide 1:1 redundancy. The switching modules from each shelf are interconnected to provide the routing and redundancy which comprises the logical stacking arrangement.

2. Regarding claim 2 – Zadikian discloses the logical stacking configuration is a closed loop stacking configuration, refer to Figures 2 and 3 and column 9 lines 25 to 42 and column 10 lines 1 to 27 and column 11 lines 45 to 67. All the switches are interconnected in a closed loop forming a matrix formation.

3. Regarding claim 3 – Zadikian discloses one switching module within the computer system is operable as a master switching module, refer to Figure 3 (system switch) and column 12 lines 30 to 42. One switch is the master and the second is the backup switch master.

4. Regarding claim 4 – Zadikian discloses any switching module within the computer system is operable as the master switching module, refer to Figures 1A and 2-4 and column 9 lines 9 to 18.

5. Regarding claim 5 – Zadikian discloses only one switching module within the computer system operates as a master switch at any given time, refer to Figure 3 (system switch) and column 12 lines 30 to 42. One switch is the master and the second is the backup switch master.

6. Regarding claim 6 – Zadikian discloses all switching modules in the computers system other than the master switching module are operable as slave switching modules responsive to the master switching module, refer to Figures 1A and 2-4 and column 9 lines 9-18 and column 12 lines 30 to 42.

7. Regarding claim 7 – Zadikian discloses the shelves are logically connected into a plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in a logical stacking configuration, wherein the computer system further comprises a master shelf including a carrier for removably receiving a master switching module, wherein the master switching module is connected into each stack as a common master switch for all of the stacks, wherein the master switching module is connected to the switching module of a first shelf and to the switching module of a last shelf in each of the stacks, refer to Figures 1A, 2-4 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36. Radian discloses a rack with comprises shelves and a backplane within each shelf comprises line cards, processor cards, and switch cards. The cards are interconnected to provide 1:1 redundancy. The switching modules from each shelf are interconnected to provide the routing and redundancy which comprises the logical stacking arrangement. Zadikian discloses that multiple racks are used for scalability, refer to Figure 9 and column 16 lines 28 to 50.

8. Regarding claim 8 – Zadikian discloses a system management module configured to provide system- level management functionality to the shelves in the stacks, wherein each shelf

is coupled to the system management module via a management connection, refer to Figures 1A and column 8 lines 55 to 67.

9. Regarding claim 9 – Zadikian discloses a system management module coupled to the master switching module via one or more management connections, wherein the system management module is configured to provide system-level management functionality to the shelves in the stacks via the master switching module, refer to Figures 1A and column 8 lines 55 to 67.

10. Regarding claim 10 – Zadikian discloses the master switching module is configured to multiplex management information from the system management module in with data content transmitted to the shelves via inter-shelf connections, refer to Figures 1A and column 8 lines 55 to 67.

11. Regarding claim 11 – Zadikian discloses each shelf comprises two switching modules removably received therein, refer to Figure 4 and column 12 lines 44 to 60.

12. Regarding claim 12 – Zadikian discloses both switching modules of each shelf are connected into a common logical stacking arrangement, refer to Figures 2 and 3 and column 9 lines 25 to 42 wherein each switch provides 1:1 redundancy.

13. Regarding claim 13 – Zadikian discloses each switching module of each shelf is connected into a different logical stacking arrangement to the other switching module of that shelf, refer to Figure 3 and column 11 line 65 to column 12 line 8. Each switch interconnects to other line cards to provide redundancy.

14. Regarding claim 14 – Zadikian discloses each shelf is connected into two logical stacking arrangements, each switching module of the shelf being connected into a different one of the logical stacking arrangements, and wherein the each logical stacking arrangements provides equivalent connectivity between the shelves as the other logical stacking arrangement, refer to Figure 3 and column 11 line 65 to column 12 line 8. Each switch interconnects to other line cards to provide redundancy.

15. Regarding claim 15 – Zadikian discloses each switching module of a given shelf is operable to replicate the functionality of the other switching module of that shelf, refer to Figures 2 and 3 and column 9 lines 25 to 42 wherein each switch provides 1:1 redundancy.

16. Regarding claim 16 – Zadikian discloses one switching module of each shelf is operable as a shelf level master switching module and wherein the other switching module of that shelf is operable as a shelf level slave switching module, refer to Figures 2 and 3 and column 9 lines 25 to 42 wherein each switch provides 1:1 redundancy.

17. Regarding claim 17 – Zadikian discloses each switching module of a given shelf is interconnected with the other switching module of that shelf, refer to Figures 2 and 3 and column 9 lines 25 to 42.

18. Regarding claim 18 – Zadikian discloses each shelf comprises two switching modules removably received therein, wherein the shelves are logically connected into a plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in at least one logical stacking configuration, wherein the computer system further comprises a master shelf including a carrier for removably receiving two master switching modules, wherein each of the master switching modules is connected into each stack as a common master switch for all of the stacks, wherein the computer system further comprises a system management module configured to provide system-level management functionality to the shelves in the stacks, refer to Figures 1A, 2-4 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36. Radian discloses a rack with comprises shelves and a backplane within each shelf comprises line cards, processor cards, and switch cards. Refer to Figure 3 and column 11 line 65 to column 12 line 8. Refer to Figures 1A and column 8 lines 55 to 67.

19. Regarding claim 19 – Zadikian discloses each shelf also comprises a service processor module for providing management functions in respect of said information processing modules, refer to Figure 4 and column 8 lines 40 to 55.

20. Regarding claim 20 – Zadikian discloses each switching module of each shelf comprises a service processor module, refer to Figure 4 and column 8 lines 40 to 55.

21. Regarding claim 21 – Zadikian discloses each switching module comprises at least one forwarding element for performing a forwarding operation and a respective controlling element for controlling the switching element, refer to Figures 1A, 2-4 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36.

22. Regarding claim 22 – Zadikian discloses each switching module comprises at least one switch fabric chip and a controlling microprocessor, and wherein the functionality of each forwarding element is performed by a switch fabric chip and the functionality of the controlling element is performed by the same switch fabric chip and the controlling microprocessor in combination, refer to Figures 1A, 2-4, 7, and 10 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36 column 15 lines 13 to 25 and column 15 lines 13 to 25.

23. Regarding claim 23 – Zadikian discloses each controlling element is aware of the topography of the stack, refer to Figures 1A, 2-4, 7, and 10 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36 column 15 lines 13 to 25 and column 15 lines 13 to 25.

24. Regarding claim 24 – Zadikian discloses each controlling element is operable to control the operation of the forwarding element to cause a unicast data element to be forwarded by its respective forwarding element using a shortest transmission path to its target, refer to column 7 lines 20 to 40.

25. Regarding claim 25 – Zadikian discloses each controlling element is operable to control the operation of the forwarding element to cause a multicast or broadcast data element to be forwarded once around the stack in a given direction, refer to column 7 line 40 to column 8 line 10.

26. Regarding claim 26 – Zadikian discloses each switching module is content aware, refer to Figures 1A, 2-4, 7, and 10 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36 column 15 lines 13 to 25 and column 15 lines 13 to 25.

27. Regarding claim 27 – Zadikian discloses the controlling element is operable to study a transmitted data element to determine a path to destination based on the content of that data element, refer to the abstract and column 3 line 1 to 25.

28. Regarding claim 28 – Zadikian discloses a plurality of shelves, each shelf including a carrier for removably receiving a plurality of information processing modules and a switching module, and an interconnection member for providing connections between the information processing modules and the switching module, wherein the shelves are logically connected into a

plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in a logical stacking configuration, a master shelf including a carrier for removably receiving a master switching module, wherein the master switching module is connected into each stack as a common master switch for all of the stacks; and a system management module coupled to the master switching module and to an external management network via a plurality of management connections, wherein the system management module is configured to provide system-level management functionality to the shelves in the stacks via the master switching module, refer to refer to Figures 1A, 2-4 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36. Radian discloses a rack with comprises shelves and a backplane within each shelf comprises line cards, processor cards, and switch cards. Refer to Figure 3 and column 11 line 65 to column 12 line 8. Refer to Figures 1A and column 8 lines 55 to 67.

29. Regarding claim 29 – Zadikian discloses a plurality of shelves, each shelf including a carrier for removably receiving a plurality of information processing modules and at least one switching module, and an interconnection member for providing connections between the information processing modules and the at least one switching module; wherein each switching module of each shelf comprises at least one forwarding element for performing a forwarding operation and a respective controlling element for controlling the switching element; wherein each switching module of each shelf comprises at least one switch fabric chip and a controlling microprocessor, and wherein the functionality of each forwarding element is performed by a switch fabric chip and the functionality of the controlling element is performed by the same

switch fabric chip and the controlling microprocessor in combination, refer to Figures 1A, 2-4 and column 9 line 25 to 42 and column 10 lines 10 to 27 and column line 45 to column 13 line 36. Radian discloses a rack with comprises shelves and a backplane within each shelf comprises line cards, processor cards, and switch cards. Refer to Figure 3 and column 11 line 65 to column 12 line 8. Refer to Figures 1A and column 8 lines 55 to 67.

Response to Arguments

Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Colton (US 2005/0089027 A1) discloses intelligent optical data switching system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel, can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C.

or faxed to:

(571) 273-8300

For informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

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Alexandria, VA, 22313.

John Pezzlo

28 September 2007

JOHN PEZZLO
PRIMARY EXAMINER